1,068,199

PATENT SPECIFICATION 1,068,199

DRAWINGS ATTACHED.

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Int. Cl.:—H 01 l 7/50.

COMPLETE SPECIFICATION.

High Voltage Semiconductor Device.

We, INTERNATIONAL RECTIFIER CORPORATION, a corporation organized and existing under the laws of the State of California, United States of America, of 233 Kansas Street, El Segundo, California, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a semiconductor structure and method of manufacture thereof for the formation of junctions capable of withstanding high reverse voltages.

A primary object of this invention is to provide an improved high voltage semiconductor device.

A further object of this invention is to increase the creepage distance across the effective edge of a wafer.

Yet another object of this invention is to increase the effective distance between the metallic electrodes of a semiconductor device.

According to the invention there is provided a semiconductor wafer having at least one planar junction therein and extending completely through the wafer and terminating at the edge thereof, first and second thin flat electrodes on respective first and second opposing surfaces thereof, and an annular groove in said first surface of said wafer, said annular groove extending through at least one said junction and defining a thin rim about the periphery of said wafer, and said first electrode being on the inner area of said first surface defined by said annular groove.

The invention also includes a method of treating a wafer of semiconductor material having a junction therein which extends completely through the wafer and terminates at the edge thereof comprising the steps of masking the bottom surface, sides and outer periphery of the top surface of said wafer and an inner surface area of the top surface of said area, leaving an exposed annular area at the top of said wafer, exposing said masked wafer to a first etching step to etch the beginning of an annular groove extending from the exposed annular area of said top surface of said wafer, removing and replacing said mask on said inner surface area with a smaller area mask to expose an increased annular area at the top of said wafer, and exposing said newly masked wafer to a second etching step to continue to etch said annular groove sufficient to break through at least one junction and removing and washing said wafer.

In the case of high voltage semiconductor devices, there is an aggravated problem of creepage and tracking across the edge surface of the wafer. In accordance with one form of the present invention, the effective edge surface of the wafer, namely the inner edge of the annular groove, is caused to have an angle of less than 90° with respect to the plane of the junction to thereby reduce the surface field across the junction such that the bulk avalanche break-down always occurs prior to a surface break-down. Thus, the reverse voltage withstanding ability of the junction is increased.

Moreover, the annular groove, which does not extend completely through the wafer, provides a longer surface creepage distance between the metallic electrodes of the device before hermetic sealing.

In both the specification and claims, the terms "thin" and relatively "thin" are used in relation to the rim of the wafer. It will be appreciated that in the invention it is necessary to isolate the planar edges from the rim of the wafer while keeping the available junction area as large as possible. To

do this, it is necessary that the inactive rim be made thin. By "thin" or relatively "thin" therefore we are thinking of thicknesses generally less than 100 mils, for example 40 mils.

In order that the invention may be more readily understood, embodiments thereof will now be described with reference to the accompanying drawings, in which:—

Figure 1 is a top view of a wafer which has metallic electrodes thereon, and is to be treated in accordance with the present invention.

Figure 2 is a cross-sectional view of Figure 1 taken across the lines 2—2 in Figure 1.

Figure 3 illustrates the wafer of Figure 2 contained within a jig and subjected to a first etching operation to form a first portion of an annular groove.

Figure 4 illustrates the wafer of Figure 3 contained within a second jig structure for the completion of the etching operation.

Figure 5 shows the finished wafer after the operation of Figure 4 and the placement of varnish in the finished groove.

Figure 6 is a top view of Figure 5.

Figure 7 shows an enlarged view of the groove of Figure 5.

Referring first to Figures 1 and 2, we have shown therein a semiconductor wafer 10 which could, for example, be of silicon, and could have a junction 11 therein formed between an N-type lower surface region and P-type upper surface region. Alternatively, the upper surface region could be N and the lower surface region P. It is to be particularly understood that while the invention is illustrated by the case of a semiconductor device having a single junction 11, a device having any number of junctions could have been presented herein. For the case of the illustrative wafer, however, it may be presumed that the junction 11 is formed between a lower N-type region and upper P-type region, and can be formed in any desired manner as by diffusion, alloying, epitaxial techniques, and so on.

The wafer is further shown to have formed thereon upper and lower electrodes 12 and 13 which could be applied to the wafer in any desired manner.

For purposes of illustration, the wafer of Figures 1 and 2 could, for example, have a diameter of 700 mils and a thickness, for example, of 14 mils. The resistivity of the material may be of any desired value, depending upon the end use of the product.

The object of the present invention is to operate upon the wafer of Figures 1 and 2 in such a manner as to shape the ends of junction 11 to cause the junction to have improved reverse voltage characteristics and to provide an increased effective distance between the junction and any metallic parts such as electrodes 12 and 13.

The wafer is initially cleaned in a suitable manner, and is thereafter assembled within a jig of the type shown in Figure 3. More specifically, the jig of Figure 3 includes a first masking section 20 of suitable acid-resistant material such as "Teflon" (Registered Trade Mark) (polytetrafluoroethylene) which completely encloses the sides and bottom of the wafer along with a small annular region of the wafer extending in from the edge thereof. By way of example, the diameter of the opening of jig 20 may be 620 mils so that an annular band having a radial thickness of 40 mils extending inwardly from the edge of the wafer is covered. A second mask 21 is then applied to cover or mask a central area of the upper surface of the wafer which could, for example, have a diameter of 560 mils. It is to be noted that the external mask 20 could be replaced by any suitable masking medium which would prevent an etching material from contacting any of the surface covered by the jig 20. The mask 21, however, is preferably an easily removable masking structure since, as will be seen more fully hereinafter, it must be quickly removed and replaced by a smaller diameter mask during a subsequent step of the etching operation.

Once the wafer is suitably masked, as illustrated in Figure 3, the wafer is dipped into an etching compound which will cause the etching of an annular groove 22 which extends just through the junction 11. By way of example, the junction 11 could be $3\frac{1}{2}$ mils beneath the upper surface of wafer 10 so that the first etch can extend to about 4 mils in depth. A typical etching medium is formed of three parts nitric acid, one part hydrofluoric acid and one part acetic acid. The groove 22 will be etched in approximately 4 minutes at room temperature. Clearly, this time depends on the exact location of junction 11 within the wafer and thus the depth to which the etch must extend.

Thereafter, the wafer and jig are quickly removed from the etching medium, and the upper mask 21 is removed and replaced by a second mask 23, as illustrated in Figure 4. The mask 23 of Figure 4 will have a diameter, for example, of 425 mils and the newly masked structure is then returned to the etching medium. After approximately $2\frac{1}{2}$ minutes at room temperature, the new groove 24 will be formed wherein the newly exposed regions of semiconductor material will now be etched to assume the shape as shown in Figure 4, and particularly as shown in Figure 7. It is to be specifically noted that this etch is stopped prior to the complete etch through the wafer 10 so that the lower electrode 13 is not exposed to the etch. By way of example, the thickness of wafer 10 left at the base of wafer 24 could be 1 mil.

The specific angle θ formed by tangent line 30 to the inner wall of the groove at the plane of the junction in Figure 7 with respect to the plane of junction 11 is less than 90°, but its exact magnitude will depend on the resistivity of the material used, which, in turn, determines avalanche break-down voltage, and the desired rated voltage of the device. Higher resistivities will give a greater space charge spread for a given voltage so the angle θ preferably decreases as resistivity increases so the surface field is correspondingly reduced. For example, for a 40 ohm centimeter resistivity, avalanche break-down is at the order of 1500 volts and an angle θ of the order of 45° would be used and generally θ will lie in the range of between 10° and 60°.

Once the second etch is completed, the wafer is removed from the etching compound, and is washed and cleaned with distilled water at room temperature. Thereafter, a final cleaning operation with distilled water is used.

It is to be further noted that the final product, as shown in Figure 5, is one in which there will be very low surface leakage across the effective edge of the wafer which is the inner diameter of groove 24, because of the shaping operating which gives a smooth and clean surface. Moreover, this surface is completely isolated from the lower metallic electrode 13 by virtue of the remaining wafer rim section external of groove 24. Moreover, the contoured surface has been found to have considerably improved reverse voltage-withstanding capability.

After the successful formation of groove 24, the finished wafer may be coated with a suitable varnish which fills the groove 24, as illustrated by the varnish 31 in Figure 5. This coating step may be eliminated where the wafer can be subsequently mounted in a suitably inert atmosphere. Thereafter, the wafer may be assembled into a completed device having terminals 32 and 33 applied to electrodes 12 and 13 and the device encased in a suitable housing.

WHAT WE CLAIM IS:—

1. A semiconductor wafer having at least one planar junction therein and extending completely through the wafer and terminating at the edge thereof, first and second thin flat electrodes on respective first and second opposing surfaces thereof, and an annular groove in said first surface of said wafer, said annular groove extending through at least one said junction and defining a thin rim about the periphery of said wafer, and said first electrode being on the inner area of said first surface defined by said annular groove.

2. A semiconductor wafer having at least one planar junction therein which extends completely through the wafer and terminates at the edge thereof and at least a first and second electrode on the respective first and second opposing surfaces thereof, and an annular groove in said first surface of said wafer, said annular groove extending through said junction and defining a relatively thin rim about the periphery of said wafer, and said first electrode being on the inner area of said first surface defined by said annular groove, said groove having a configuration whereby a tangent line to the inner wall of said groove at its intersection with said junction is at an angle less than 60° with respect to the plane of said junction.

3. A semiconductor wafer as claimed in Claim 1 or 2, wherein said angle is in the range of 10° to 60°.

4. A semiconductor wafer as claimed in any preceding claim, wherein said rim has a radial thickness of substantially 40 mils.

5. A semiconductor wafer as claimed in any preceding claim, wherein said groove has a depth which extends to substantially 1 mil from said second surface.

6. A semiconductor wafer as claimed in any preceding claim, wherein said groove is filled with an electrically inert material.

7. A method of treating a wafer of semiconductor material having a junction therein which extends completely through the wafer and terminates at the edge thereof comprising the steps of masking the bottom surface, sides and outer periphery of the top surface of said wafer and an inner surface area of the top surface of said area, leaving an exposed annular area at the top of said wafer, exposing said masked wafer to a first etching step to etch the beginning of an annular groove extending from the exposed annular area of said top surface of said wafer, removing and replacing said mask on said inner surface area with a smaller area mask to expose an increased annular area at the top of said wafer, and exposing said newly masked wafer to a second etching step to continue to etch said annular groove sufficient to break through at least one junction and removing and washing said wafer.

8. The method of Claim 7, wherein said first etching step is discontinued only after said groove reaches said junction.

9. The method of Claim 8, wherein said second etching step is discontinued just before said groove reaches the bottom of said wafer.

10. The method of Claim 7, wherein said second etching step is discontinued only after the walls of said groove form a predetermined angle at the point at which they intersect said junction.

11. A semiconductor wafer substantially

as herein described with reference to the accompanying drawings.

12. The method of treating a semiconductor wafer substantially as herein described with reference to the accompanying drawings.

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1068199 COMPLETE SPECIFICATION

1 SHEET *This drawing is a reproduction of the Original on a reduced scale*

FIG. 1.

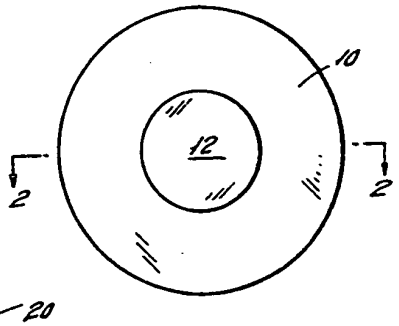

FIG. 2.

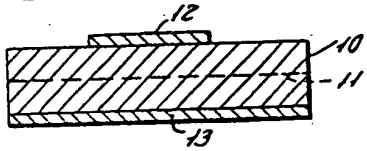

FIG. 3.

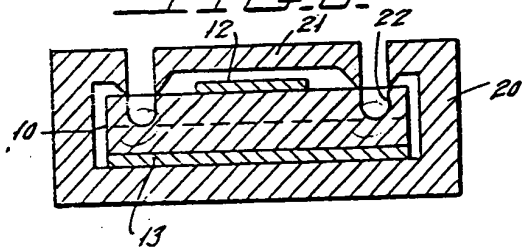

FIG. 4.

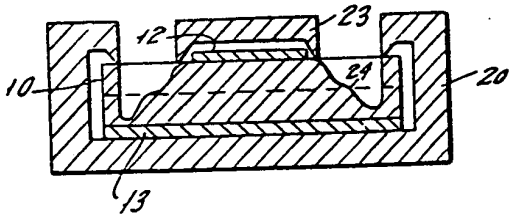

FIG. 5.

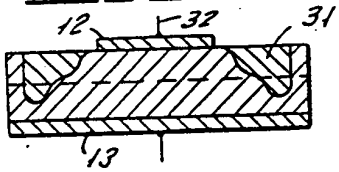

FIG. 6.

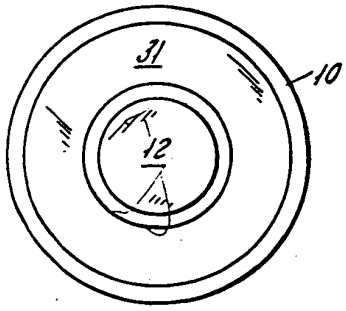

FIG. 7.